What is claimed is:

1. A Gray code counter comprising:

a consecutively counting Gray code counter that counts in increments or decrements of one; and

an output value converter circuit,

wherein the output value converter circuit converts Gray code data output from the consecutively counting Gray code counter into a Gray code corresponding to a decimal count as obtained by counting with (2 raised to a particular power minus 1) counts skipped at a time.

2. A Gray code counter as claimed in claim 1,

wherein the consecutively counting Gray code counter is an N-bit counter, and

when counting is performed with $2^M - 1$ counts skipped at a time, the output value converter circuit operates in such a way as to

output highest $(N-M)$ bits

by using, as data of an $(\alpha + M)$th bit, data of an αth bit belonging to lowest $(N-M)$ bits of the Gray code data output from the consecutively counting Gray code counter, and

output remaining lowest M bits

by inverting data of an $(M-1)$th bit every time a count changes, and

by keeping data of $(M-2)$th and lower bits, if any, constant at "0."

3. A Gray code counter as claimed in claim 1, further comprising an input value converter circuit and a count start data setting circuit,

wherein, when counting is performed with a predetermined number of counts skipped

at a time, the input value converter circuit converts, according to the number of counts skipped, Gray code data corresponding to a decimal count at which to start counting into a Gray code corresponding to a decimal count as obtained when counting is performed consecutively, and

the count start data setting circuit controls an initial state of the consecutively counting Gray code counter according to the Gray code data output from the input value converter circuit.

4. A Gray code counter as claimed in claim 3,

wherein the consecutively counting Gray code counter is an N-bit counter, and

when counting is performed with $2^M - 1$ counts skipped at a time, the output value converter circuit operates in such a way as to

output highest $(N - M)$ bits

by using, as data of an $(\alpha + M)$th bit, data of an αth bit belonging to lowest $(N - M)$ bits of the Gray code data output from the consecutively counting Gray code counter, and

output remaining lowest M bits

by inverting data of an $(M - 1)$th bit every time a count changes, and,

if an $(M - 2)$th or any lower bit exists, by using, as data of a βth bit, data of a βth bit belonging to $(M - 2)$th and lower bits of Gray code data output from the consecutively counting Gray code counter when counting is started.

5. A Gray code counter as claimed in claim 1,

wherein the output value converter circuit comprises a selector circuit, and,

according to an external signal, the selector circuit chooses whether

to output the Gray code data output from the consecutively counting Gray code counter intact or

to convert the Gray code data output from the consecutively counting Gray code counter into a Gray code corresponding to a decimal count as obtained by counting with (2 raised to a particular power minus 1) counts skipped at a time.

6. A Gray code counter as claimed in claim 2,

wherein the output value converter circuit comprises a selector circuit, and,

according to an external signal, the selector circuit chooses whether

to output the Gray code data output from the consecutively counting Gray code counter intact or

to convert the Gray code data output from the consecutively counting Gray code counter into a Gray code corresponding to a decimal count as obtained by counting with (2 raised to a particular power minus 1) counts skipped at a time.

7. A Gray code counter as claimed in claim 3,

wherein the output value converter circuit comprises a selector circuit, and,

according to an external signal, the selector circuit chooses whether

to output the Gray code data output from the consecutively counting Gray code counter intact or

to convert the Gray code data output from the consecutively counting Gray code counter into a Gray code corresponding to a decimal count as obtained by counting with (2 raised to a particular power minus 1) counts skipped at a time.

8. A Gray code counter as claimed in claim 4,

wherein the output value converter circuit comprises a selector circuit, and,

according to an external signal, the selector circuit chooses whether

to output the Gray code data output from the consecutively counting Gray code counter intact or

to convert the Gray code data output from the consecutively counting Gray code counter into a Gray code corresponding to a decimal count as obtained by counting with (2 raised to a particular power minus 1) counts skipped at a time.

9. A solid-state image sensor comprising:

a plurality of photoelectric conversion elements;

a scanning circuit having a Gray code counter for sequentially reading signals from the photoelectric conversion elements,

wherein the Gray code counter is a Gray code counter as claimed in claim 5.

10. A solid-state image sensor as claimed in claim 9,

wherein the consecutively counting Gray code counter is an N-bit counter, and

when counting is performed with $2^M - 1$ counts skipped at a time, the output value converter circuit operates in such a way as to

output highest $(N - M)$ bits

by using, as data of an $(\alpha + M)$th bit, data of an αth bit belonging to lowest $(N - M)$ bits of the Gray code data output from the consecutively counting Gray code counter, and

output remaining lowest M bits

by inverting data of an $(M-1)$th bit every time a count changes, and

by keeping data of $(M-2)$th and lower bits, if any, constant at "0."

11. A solid-state image sensor as claimed in claim 9,

wherein the Gray code counter further comprises an input value converter circuit and a count start data setting circuit, so that,

when counting is performed with a predetermined number of counts skipped at a time, the input value converter circuit converts, according to the number of counts skipped, Gray code data corresponding to a decimal count at which to start counting into a Gray code corresponding to a decimal count as obtained when counting is performed consecutively, and

the count start data setting circuit controls an initial state of the consecutively counting Gray code counter according to the Gray code data output from the input value converter circuit.

12. A solid-state image sensor as claimed in claim 11,

wherein the consecutively counting Gray code counter is an N-bit counter, and

when counting is performed with $2^M - 1$ counts skipped at a time, the output value converter circuit operates in such a way as to

output highest $(N-M)$ bits

by using, as data of an $(\alpha + M)$th bit, data of an αth bit belonging to lowest $(N-M)$ bits of the Gray code data output from the consecutively counting Gray code counter, and

output remaining lowest M bits

by inverting data of an $(M-1)$th bit every time a count changes, and,

if an $(M-2)$th or any lower bit exists, by using, as data of a βth bit, data of a βth bit belonging to $(M-2)$th and lower bits of Gray code data output from the consecutively counting Gray code counter when counting is started.

13. A camera system comprising:

a solid-state image sensor;

an optical lens system for picking up an optical real image as a target of image sensing and imaging the optical real image on the solid-state image sensor;

an output circuit for producing a drive signal based on a signal output from the solid-state image sensor; and

a display device for displaying an image by being driven by the drive signal,

wherein the solid-state image sensor is a solid-state image sensor as claimed in claim 9.

14. A camera system as claimed in claim 13,

wherein the consecutively counting Gray code counter is an N-bit counter, and

when counting is performed with $2^M - 1$ counts skipped at a time, the output value converter circuit operates in such a way as to

output highest $(N-M)$ bits

by using, as data of an $(\alpha + M)$th bit, data of an αth bit belonging to lowest $(N-M)$ bits of the Gray code data output from the consecutively counting Gray code counter, and

output remaining lowest M bits

by inverting data of an $(M-1)$th bit every time a count changes, and

by keeping data of $(M-2)$th and lower bits, if any, constant at "0."

15. A camera system as claimed in claim 13,

wherein the Gray code counter further comprises an input value converter circuit and a count start data setting circuit, so that,

when counting is performed with a predetermined number of counts skipped at a time, the input value converter circuit converts, according to the number of counts skipped, Gray code data corresponding to a decimal count at which to start counting into a Gray code corresponding to a decimal count as obtained when counting is performed consecutively, and

the count start data setting circuit controls an initial state of the consecutively counting Gray code counter according to the Gray code data output from the input value converter circuit.

16. A camera system as claimed in claim 15,

wherein the consecutively counting Gray code counter is an N-bit counter, and

when counting is performed with $2^M - 1$ counts skipped at a time, the output value converter circuit operates in such a way as to

output highest $(N-M)$ bits

by using, as data of an $(\alpha + M)$th bit, data of an αth bit belonging to lowest $(N-M)$ bits of the Gray code data output from the consecutively counting Gray code counter, and

output remaining lowest M bits

by inverting data of an $(M-1)$th bit every time a count changes, and,

if an $(M-2)$th or any lower bit exists, by using, as data of a βth bit,

data of a βth bit belonging to $(M - 2)$th and lower bits of Gray code data output from the consecutively counting Gray code counter when counting is started.